REMARKS

Claims 1-61 are pending in this application. In the Office Action dated September 10, 2003, the Examiner took the following action: (1) rejected claims 25-27, 29, 32-36, 38-40, 46-50, 52-54 and 60-61 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,308,322 to Serocki *et al.*; (2) rejected claims 1-4, 6-8, 13-15 and 17-24 under 35 U.S.C. § 103(a) as being obvious over the patent to Serocki *et al.* in view of U.S. Patent No. 5,765,037 to Morrison *et al*; (3) rejected claims 5, 12 and 16 under 35 U.S.C. § 103(a) as being obvious over the patent to Serocki *et al.* in view of U.S. Patent No. 5,765,037 to Morrison *et al.*, as applied to claims 1 and 15 above, and in further view of U.S. Patent No. 6,272,599 to Prasanna; (4) rejected claims 9-11 under 35 U.S.C. § 103(a) as being obvious over the patent to Serocki *et al.*, in view of the patent to Morrison *et al.*, as applied to claim 1 above, and in further view of U.S. Patent Application No. 2002/0078268 to Lasserre; (5) rejected claims 28, 37, 45 and 51 under 35 U.S.C. § 103(a) as being obvious over the patent Serocki *et al.*, as applied to claims 25, 34 and 48 above, in view of the patent to Prasanna; (6) rejected claims 30-31, 41-44 and 55-58 under 35 U.S.C. § 103(a) as being obvious over the patent to Serocki *et al.*, as applied to claims 25, 34 and 48 above, in view of the patent application to Lasserre; and (7) rejected claim 59 under 35 U.S.C. § 103(a) as being obvious over the patent to Serocki *et al.* and the patent application to Lasserre as applied to claim 58 above further in view of the patent Prasanna.

Applicant wishes to thank Examiner Chaki for her time and courtesy in conducting a telephone interview with applicant's undersigned attorney on December 11, 2003. During the interview, applicant's attorney explained that the invention involves determining cacheability of instructions at the time the instructions are compiled, and then marking the compiled instructions according to the determination. According to one aspect of the invention, the markings can be used during execution of the compiled instructions to determine whether the compiled instruction should be cached.

Applicant's attorney then explained that marking instructions based on whether or not they should be cached and then using those markings during execution to cache instructions is markedly different from either branch prediction or re-ordering program instructions for more efficient processing. Specifically, branch prediction, as disclosed in the Serocki *et al.* patent,

involves analyzing a program as it is being executed to predict what branch will be taken, and then marking an instruction ahead of the branch with a hint corresponding to the target address of instructions in the branch that is predicted to be followed when the branch is reached. Once the prediction is made, the target addresses added to the instructions are used to prefetch instructions in the predicted branch. However, branch prediction has nothing to do with determining whether or not to cache instructions or even whether the instructions should be fetched from cache memory or from system memory. If the instruction in the predicted branch is stored in cache, the instruction is fetched from cache. If the instruction in the predicted branch is not stored in cache, the instruction is fetched from system memory. But the hints or target addresses added to the instructions do not determine whether or not the instructions are fetched from cache. In contrast, in the invention, cacheability markings added to the instructions determine whether or not the instructions are stored in cache regardless of whether or not the program containing the instructions includes branches.

After this explanation was provided, the portions of the Serocki *et al.* patent relied on for the rejections were examined in detail. It was recognized that the portion of the specification in column 8, lines 14-41 simply describes marking instructions with hints containing the target address of a predicted branch, but does not determine whether the instruction is fetched from cache or from system memory. While line 37 does refer to cache memory, that is for the purpose of explaining that the instructions instrumented with hints indicative of the most likely target addresses should not be inserted in the program too far in advance of the branch because, if the instruction happens to be stored in cache, the instruction may be overwritten with other instructions. However, the patent does not state or imply that the hints in any way determine whether the instruction is fetched from cache or system memory. A cache memory is also referred to in column 3. However, that reference to cache memory simply explains that if an instruction in a predicted branch is stored in cache when the instruction is initially executed, the instruction may be overwritten by the time the branch is reached again.

Applicant has reviewed the Serocki *et al.* patent in detail and had been unable to find any portion of the specification where the cacheability of instructions is discussed. Instead, the anticipation rejections are apparently based on the contention that "selecting of a target address for branch heuristic optimization" is "equivalent to cacheability determineations."

However, to anticipate a claim, the prior art reference must disclose every element of the claim exactly as claimed. An argument of equivalency, even if it were correct (which it is not, in this case), cannot support an anticipation rejection.

After the explanation was made by applicant's attorney, the Examiner agreed that the claim rejections based on the Serocki *et al.* patent did not seem to be justified and should therefore be withdrawn.

As previously explained, the patent to Morrison *et al.* discloses a technique for more efficiently executing branched instructions in a program by changing the order of the instructions in the program prior to execution. The program is examined during compilation to determine how long it would require to execute each instruction (its "IFT"). The instructions are then re-ordered based on the determined IFTs. While the computer system disclosed in the Morrison *et al.* patent includes a data cache and an instruction cache, the patent does not suggest how or when cacheability determinations are made. They are presumably made in a conventional manner based on how frequently the instructions are executed.

After agreeing that the rejections did not appear to be justified, the Examiner requested applicant to file this response requesting reconsideration of the rejections. Insofar as alll of the claims in the application are clearly allowable, favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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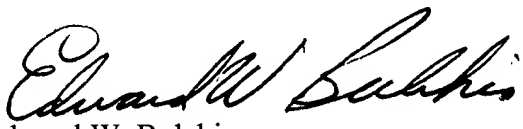

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